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Description

[METHOD OF MANUFACTURING NMOS TRANSISTOR WITH P-TYPE GATE]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92126145, filed September 23, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The present invention relates to a method of manufacturing a semiconductor device. More particularly, the present invention relates to a method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with a P-type gate.

[0004] Description of the Related Art

[0005] Metal-oxide-semiconductor (MOS) transistor is one of the most important electronic devices in a very large scale integrated (VLSI) circuit. As the name metal-oxide-semiconductor suggests, a MOS transistor is con-

sisted of three basic materials, namely, metal, oxide and semiconductor. However, modern MOS devices often use polysilicon instead of metal to contact with the oxide layer. Furthermore, a minute amount of dopants is also implanted into the polysilicon layer to lower resistivity to improve its electrical performance. Therefore, a MOS transistor should be regarded as an electronic device constructed using a doped polysilicon layer, a silicon dioxide layer and a silicon substrate.

[0006] In general, MOS devices can be classified into three major types including N-channel MOS, P-channel MOS and complementary MOS. The N-channel MOS (NMOS) can be further sub-divided into P-gate NMOS and N-gate NMOS according to the type of dopants implanted into the polysilicon layer. In dynamic random access memory (DRAM) devices, NMOS transistors are frequently used as access switches.

[0007] In recent years, advance in semiconductor fabrication technologies has produced devices with feature size down in the sub-micron regime. However, as the dimension of the devices on each chip shrinks so that the gate length of each device is reduced, short channel effect has become an increasingly important, a factor affecting the normal

operation of a MOS device. To suppress the short channel effect due to a reduction in gate length, more dopants are implanted into the channel. Yet, an over-abundant supply of dopants inside the channel may lead to an increase in leakage current. When the MOS devices are used as basic elements inside, say, a DRAM unit, too much leakage current may compromise the data retention capacity.

[0008] In a conventional DRAM device, a DRAM device using P-gate NMOS transistors require 25% less channel dopants than a DRAM device using N-gate NMOS transistors. In other words, the probability of having a leakage current resulting in a drop in data retention capacity is lowered when P-gate NMOS transistors are used. Another advantage of reducing the channel dopants is a lowering of the electric field strength at a depth roughly 0.4μm below the top surface of the substrate. However, in the fabrication of a conventional P-gate NMOS, boron ions are typical dopants implanted into the polysilicon layer. During the implantation, some of the energetic ions may break up the crystal to produce lattice defects. In addition, boron ions are also a source that aggravates the leakage problem. Therefore, using boron implantation to form P-gate NMOS transistor often has adverse effects on overall electrical

performance of the device.

SUMMARY OF INVENTION

[0009] Accordingly, one objective of the present invention is to provide a method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with a P-type gate that can improve overall electrical performance.

[0010] Another objective of this invention is to provide a method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with a P-type gate that can reduce the number of crystal lattice defects in a polysilicon layer.

[0011] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with a P-type gate. First, a substrate is provided. A gate dielectric layer is formed over the substrate. Thereafter, an indium doped polysilicon layer is formed over the gate dielectric layer. The indium doped polysilicon layer and the gate dielectric layer are patterned to form a gate. Finally, an N-doped region is formed in the substrate on each side of the gate to form the P-type gate NMOS transistor.

[0012] According to one preferred embodiment of this invention, the aforementioned method further comprises forming a metal silicide layer over the indium doped polysilicon layer after forming the indium doped polysilicon layer over the gate dielectric layer but before forming patterning the indium doped polysilicon layer and the gate dielectric layer.

[0013] In the polysilicon doping process of this invention, indium ions are used instead of the conventional boron ions. Hence, problems caused by boron ions diffusing into the substrate to affect device performance are avoided.

[0014] This invention also provides an alternative method of manufacturing an N-channel metal-oxide-semiconductor (NMOS) transistor with a P-type gate. First, a substrate is provided. A gate dielectric layer is formed over the substrate. Thereafter, an indium doped polysilicon layer is formed over the gate dielectric layer. The indium doped polysilicon layer is formed in an in-situ doping operation using indium chloride ($InCl_3$) as a source of gaseous dopants. The indium doped polysilicon layer and the gate dielectric layer are patterned to form a gate. Finally, an N-doped region is formed in the substrate on each side of the gate to form the P-type gate NMOS transistor.

[0015] According to one preferred embodiment of this invention,

the aforementioned method further comprises forming a metal silicide layer over the indium doped polysilicon layer after forming the indium doped polysilicon layer over the gate dielectric layer but before forming patterning the indium doped polysilicon layer and the gate dielectric layer.

[0016] In the aforementioned polysilicon fabrication process, indium ions are doped into the polysilicon layer in an in-situ operation. Hence, the number of lattice defects within the crystalline polysilicon layer is greatly reduced. Furthermore, because chlorine form a relatively strong bond with silicon oxide, using gaseous indium chloride as a source of dopants in the in-situ doping of polysilicon increases the bonding strength between the polysilicon layer and the gate dielectric layer.

[0017] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0018] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, to-

gether with the description, serve to explain the principles of the invention.

[0019] Figs. 1A through 1F are schematic cross-sectional views showing the progression of steps of manufacturing an NMOS transistor with a P-type gate according to one preferred embodiment of this invention.

DETAILED DESCRIPTION

[0020] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0021] Figs. 1A through 1F are schematic cross-sectional views showing the progression of steps of manufacturing an NMOS transistor with a P-type gate according to one preferred embodiment of this invention. As shown in Fig. 1A, a substrate 100 such as a P-type substrate is provided. A gate dielectric layer 102 is formed over the substrate 100. The gate dielectric layer 102 is a silicon oxide layer formed, for example, by performing a thermal oxidation process. Obviously, the gate dielectric layer 102 can be fabricated from some other dielectric material using a dif-

ferent fabricating method.

[0022] As shown in Fig. 1B, an indium doped polysilicon layer 104 is formed over the gate dielectric layer 102 and then a metal silicide layer 106 is formed over the indium doped polysilicon layer 104. To form the indium doped polysilicon layer 104, a chemical vapor deposition is performed to form an undoped polysilicon layer. Thereafter, an ion implantation is carried out implanting indium ions into the undoped polysilicon layer. Finally, an annealing operation is carried out so that the indium doped polysilicon layer 104 undergoes an internal reorganization to reduce the number of defects within the crystal lattice.

[0023] The indium doped polysilicon layer 104 can also be formed by carrying out a chemical vapor deposition with in-situ doping of indium ions. In the in-situ doping process, indium chloride ($InCl_3$) and silicane (SiH_4) are used as gaseous reactants and nitrogen and argon are used as gas carriers in the chemical vapor deposition process, for example. To form the indium doped polysilicon layer 104, solid indium chloride is heated to a temperature higher than its sublimation temperature (for example, 280°C) so that solid indium chloride vaporizes to form a gas. Thereafter, gaseous indium chloride is channeled into a chemi-

cal vapor deposition chamber where indium ions and polysilicon are deposited over the gate dielectric layer 102 in situ. In addition, the metal silicide layer 106 can be a refractory silicide compound such as tungsten silicide. The metal silicide layer 106 is formed, for example, by performing a chemical vapor deposition operation.

[0024] As shown in Fig. 1C, the gate dielectric layer 102, the indium doped polysilicon layer 104 and the metal silicide layer 106 are patterned to form a gate structure 108. The gate dielectric layer 102, the indium doped polysilicon layer 104 and the metal silicide layer 106 are patterned, for example, by conducting a photolithographic and an etching process in sequence.

[0025] As shown in Fig. 1D, N-type dopants are implanted into the substrate 100 on each side of the gate structure 108 to form lightly doped regions 110. The lightly doped regions 110 serve as lightly doped drain (LDD) regions in the subsequently formed MOS device. The lightly doped regions 110 are formed, for example, by performing an ion implantation.

[0026] As shown in Fig. 1E, spacers 112 are formed on the sidewalls of the gate structure 108 such that the spacers 112 also cover a portion of the lightly doped regions 110. The

spacers 112 are formed, for example, by performing a chemical vapor deposition to produce a dielectric layer (not shown) over the substrate 100 and then performing an anisotropic etching operation to remove a portion of the dielectric layer.

[0027] As shown in Fig. 1F, N-type dopants are implanted into the substrate 100 on each side of the gate structure 108 just outside the spacers 112 to form heavily doped regions 110a. Here, the process for fabricating a P-type gate NMOS transistor is completed. The heavily doped regions 110a are formed, for example, by performing an ion implantation. Each heavily doped region 110a together with a corresponding lightly doped region 110 form a source/drain region 114.

[0028] In the aforementioned P-type gate NMOS transistor, the metal silicide layer serves to lower the resistivity of the gate structure and hence its presence is not absolutely essential. In this invention, one may choose to form a metal silicide layer over the indium doped polysilicon layer.

[0029] In this invention, an indium doped polysilicon layer replaces the conventional boron doped polysilicon layer as the gate for the NMOS transistor. Since indium ions are

harder to diffuse, the P-type gate NMOS transistor has a better electrical performance than the conventional P-type gate NMOS transistor.

[0030] It is to be noted that the indium doped polysilicon layer may be formed by performing an in-situ chemical vapor deposition process. Because a doped polysilicon formed in an in-situ process requires no subsequent annealing operation, defects in the crystal lattice due to improper control of the annealing parameters can be avoided. Furthermore, using gaseous indium chloride as a doping source has the added advantage of strengthening the bond between the indium doped polysilicon layer and the silicon oxide layer (the gate dielectric layer) because chlorine atoms have great affinity for silicon oxide.

[0031] Furthermore, the P-type gate NMOS transistor of this invention can be applied to form a dynamic random access memory (DRAM). The P-type gate NMOS transistor of this invention is able to boost the data retention capacity of the DRAM because the indium doped polysilicon layer has greater capacity than the conventional boron doped polysilicon layer to prevent leakage.

[0032] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure

of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.